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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/467,675 | 12/21/1999 | FU-TAI LIOU | 252103-4540 | 2680 |

7590 06/30/2004

J.C. PATENT
4 VENTURE
SUITE-250
IRVINE, CA 92618

| EXAMINER | |
|---|---|
| NADAV, ORI | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Offic Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 09/467,675 | LIOU ET AL. |
| | Examiner | Art Unit |
| | ori nadav | 2811 |

*-- The MAILING DATE of this communication appears on the cover she t with th correspondence address --*

**Peri d f r Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *23 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-16 and 19-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 19-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim R j ctions - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-16 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Swonger (5,663,860) in view of Hwang et al. (5,273,915) and Yamaguchi et al. (6,118,154).

Swonger teaches in figure 4 and related text an ESD protection structure having a silicon sided diode used to protect an internal circuit, the ESD protection structure electrically connected between an input pad 31 (see figure 5), 12 and a node 14 and the internal circuit electrically connected to the node, the ESD structure comprising;

an input resistor Rpin including a plurality of resistors 13a, 13b formed over an insulating material layer 42 comprising oxide (figure 6), electrically coupled between the input pad and the node, wherein the resistors 13a, 13b are arranged in parallel connection, and

at least a single sided junction diode 26a formed over the insulating material layer 42, wherein the diode is electrically coupled between one terminal of a corresponding power supply 24 and a node 14 and dominates discharge of ESD current.

Swonger does not teach forming the device in a single crystal silicon.

Hwang et al. teach forming passive elements, including resistors, vertically and laterally isolated by dielectric material in a single crystal silicon (column 9, lines 1-25). Yamaguchi et al. teach in figure 22 forming a single crystal silicon sided junction diode 38.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form Swonger's device (including the diodes and the resistors) in a single crystal silicon, such that the diodes and the resistors are vertically and laterally isolated by dielectric material, as taught by Hwang et al. and Yamaguchi et al., in order to improve the characteristics of the device and to increase the breakdown voltage of the device. The combination is also motivated by the teachings of Hwang et al. who point out the advantages of using single crystal silicon resistors (column 9, lines 10-16).

Regarding claim 3, Hwang et al. and Yamaguchi et al. teach an SOI. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form Swonger's device on an SOI in order to improve the characteristics and the electrical isolation of the device.

Regarding claims 4 and 10, Swonger and Yamaguchi et al. teach an input buffer electrically coupled between the node and the internal circuit.

Regarding claims 7 and 13, Yamaguchi et al. teach a diode comprising a MOS transistor formed over the insulating layer, wherein one of the source/drain regions

electrically connects to a gate by a wire line. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form Swonger's diode of MOS transistor in order to provide a diode having improved characteristics by a well-known method.

Regarding claim 8, Swonger teaches junction diodes comprising first and second diodes, electrically connected between the node and one terminal of a first and second power supply, respectively.

Regarding claim 14, Yamaguchi et al. teach in figure 22 first, second and third conductive layers 13, 14, 15 formed over the insulating layer and electrically connecting the resistor between the input and the integrated circuit and the diode to the integrated circuit, respectively. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form first, second and third conductive layers over the insulating layer and electrically connecting the resistor between the input and the integrated circuit and the diode to the integrated circuit, respectively, in Swonger's device in order to operated the device in its intended use. Note that the device would not operate without electrical connections.

Regarding claim 20, it is conventional to use STI as an isolation structure, of which judicial notice is taken.

***Respons to Arguments***

3. Applicant argues that Swonger fails to teach or suggest a single crystal silicon-side junction diode electrically coupled between one terminal of a corresponding power supply and a node, because terminal 24 is actually a ground voltage reference terminal (col. 4, line 23 and col. 7, line 8) and not a power supply.

Swonger teaches a junction diode electrically coupled between one terminal of a corresponding power supply and a node, because terminal 24 can be a voltage supply (col. 4, lines 25-27).

4. Applicant argues that Swonger fails to teach or suggest a single crystal silicon-side junction diode electrically coupled between one terminal of a corresponding power supply and a node, because low voltage reference terminal 24 may more generally represent any voltage line through which discharging of high voltages appearing at pin 12 is desired, and it is impossible to discharge an ESD current through a power supply line.

Discharging of high voltages appearing at a pin through reference voltage can be considered as a discharge of an ESD current. Therefore, it is possible to discharge an ESD current through reference voltage 24, as claimed.

5. Applicant argues that diode 26a/b does not dominate discharge of ESD current.

The claimed limitation of a diode dominating discharge of ESD current includes a relative term (dominating) that under certain spiking conditions can be considered as "dominating". Note that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

**Papers related to this application may be submitted to Technology c nter (TC) 2800 by facsimile transmission. Papers should be fax d to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.**

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
June 25, 2004

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800